▼ Journal of Research (Science), Bahauddin Zakariya University, Multan, Pakistan.
Vol.13, No.1, June 2002, pp. 01-07 ISSN 1021-1012

STUDY OF ELECTRICAL PROPERTIES OF ISOTYPE GaAs(In,Ga)P/GaAs HETEROINTERFACES GROWN BY MOVPE BY CAPACITANCE-VOLTAGE AND DLTFS TECHNIQUES.

M. Asghar[1], P. Krispin[2], A. Knauer[3] and H. Kostial[2]
[1]Department of Physics, Islamia University Bahawalpur, Pakistan, [2]Paul-Drude-Institiut fur Festkorperelektronik, Hausvogteiplatz 5-7, 10117 Berlin, Germany, [3]Ferdinand-Brown-Institut fur Hoschstfrequenztechnik, Albert-Einstein-St. 11, 12489 Berlin, Germany
email: asghar_hashmi@yahoo.com

Abstract: Capacitance-voltage measurements and deep level transient Fourier spectroscopy are used to examine the depth resolved electrical characteristics of Si-doped GaAs/(In,Ga)P/GaAs heterojunctions grown by metal-organic-vapor-phase epitaxy. The depth profiles of the carrier concentration are compared with calculations based on self-consistent solutions of the Poisson equation. It is shown that the depth profiles of GaAs/(In,Ga)P interfaces depend strongly on the growth conditions. For interfaces with disordered (In,Ga)P, the conduction band offset is determined to be 0.20 eV. The estimated carrier deficits at the various heterointerfaces are within the range 10^{12} - < 10^{11} cm^{-2}. The apparent loss of carriers at the typical interface is related to the interfacial levels.

Keywords: DLTFS, electrical characteristics, InGaP/GaAs heterojunction, MOVPE.

INTRODUCTION

Aluminum free (In, Ga)P/GaAs heterojunctions are considered to be an attractive alternative to the (Al, Ga)As/GaAs material system for electronic devices. As an example the electronic devices such as heterojunction bipolar transistors (HBTs), high-electron-mobility transistors (HEMTs), light-emitting and laser diodes (LEDs and LDs) and solar cells are being frequently realized by using lattice-matched (In, Ga)P/GaAs layers. The electronic properties of the (In, Ga)P/GaAs interfaces are therefore of vital importance for potential applications of the aforesaid devices. Despite a larger number of investigations, the electrical characteristics of (In,Ga)P/GaAs heterointerfaces are still controversially discussed. The values for the conduction band offset ΔE_c obtained from the various measurement techniques range from 0.03 to 0.25 eV [Lee *et al.* 1992, Feng *et al.* 1993, Kim *et al.* 1996, O'Shea *et al.* 1996, Cai *et al.* 1999]. For the valence band offset ΔE_v, values between 0.24 and 0.40 eV have been reported in literature [Rao *et al.* 1987, Biswas *et al.* 1990, Chen *et al.* 1991]. Although it is known that (In, Ga)P exhibits a tendency to decompose and order, yet it is not clear, how this affects the electronic properties of lattice-matched (In, Ga)P/GaAs heterointerfaces grown by metal-organic-vapor-phase epitaxy (MOVPE).

Keeping in view the fact that the interfacial levels have drastic effects on the characteristics of the devices [Zhang *et al.* 1987, Krispin *et al.* 1998],

our investigations therefore, focus on Si-doped GaAs/(In, Ga)P/GaAs isotype heterointerfaces grown by MOVPE under different conditions. The electrical properties of the heterojunctions are examined by the capacitance-voltage (*C*-*V*) method [Blood and Orton 1992] and deep level transient Fourier spectroscopy (DLTFS) [Weiss and Kassing 1988]. The conduction band offset ΔE_c has been determined by one-dimensional simulation technique based on self-consistent solution of the Poisson equation [Tan *et al.* 1990]. It is shown that the free electron distribution at n-type GaAs(In, Ga)P interfaces strongly depends on the growth conditions. Secondly, the carrier deficit observed at the interface by *C*-*V* method is actually related to the interfacial and/or deep levels as seen by DLTFS measurements.

MATERIALS AND METHODS

The investigated GaAs(In, Ga)P/GaAs heterojunctions were grown by MOVPE under different conditions. The details of the growth conditions can be seen in our earlier communication [Krispin *et al.* 2000]. Briefly, the random (In,Ga)P alloys were grown at 580°C on (001)-oriented GaAs. Double- and single-variant ordered (In, Ga)P layers were realized at a growth temperature of 650°C on single and vicinal (001) substrates with a miscut of 2° towards (111)B, respectively. V/III input ratios of 70 or 140 and growth rates of 2.5 μm h^{-1} were used. The lattice mismatch of the layers in all cases, was smaller than 5×10^{-4}. The interface regions were realized by growth interruptions of about 5s. For electrical measurements, vacuum-deposited Ti/Au dots sizing 4.11×10^{-4} cm^2 and 1.58×10^{-3} cm^2, were formed as metal-semiconductor (MS) contacts and the ohmic contacts of Au-Ge alloy were provided on the backside of the substrate.

The depth profile of the apparent free carrier concentration $N_{C\text{-}V}$ was measured using the conventional method [Blood and Orton 1992]. The concentration $N_{C\text{-}V}$ was obtained from the expression:

$$N_{C-V}(W) = 2 / A^2 q \varepsilon\varepsilon_o \left[d / dV \left\{ 1 / C^2 \right\} \right]$$

Where *W* denotes the thickness of the space-charge layer below the MS contact, A the contact area, *q* the elementary charge, and $\varepsilon\varepsilon_o$ the dielectric constant. The depth *W* was calculated from the capacitance *C* using $W(V) = \varepsilon\varepsilon_o A/C(V)$. Deep levels were investigated by the DLTFS technique [Weiss and Kassing 1988], where the time transients of the capacitance *C* are digitized and the discrete Fourier coefficients are calculated at each temperature. The interface-state density N_{SS} was calculated by incorporating the DLTFS peak height $\Delta C/C$ in the expression given by Tan *et al.* [1990]:

$$N_{SS}(E) = \left[\tau \, N_{C-V} \varepsilon\varepsilon_o / (T_W C k T) \right] \Delta C / C$$

where E represents the activation energy of the interface state, τ the time constant T_W the pulse width, k the Boltzmann constant (8.862×10^{-5} eVK^{-1}), and T the temperature position of the DLTFS peak associated with the interface state.

Capacitance-voltage (C-V) measurements were performed using HP4275 LCR meter at 1 MHz. The DLTFS measurements were carried out by PC-controlled DL8000 BioRad system.

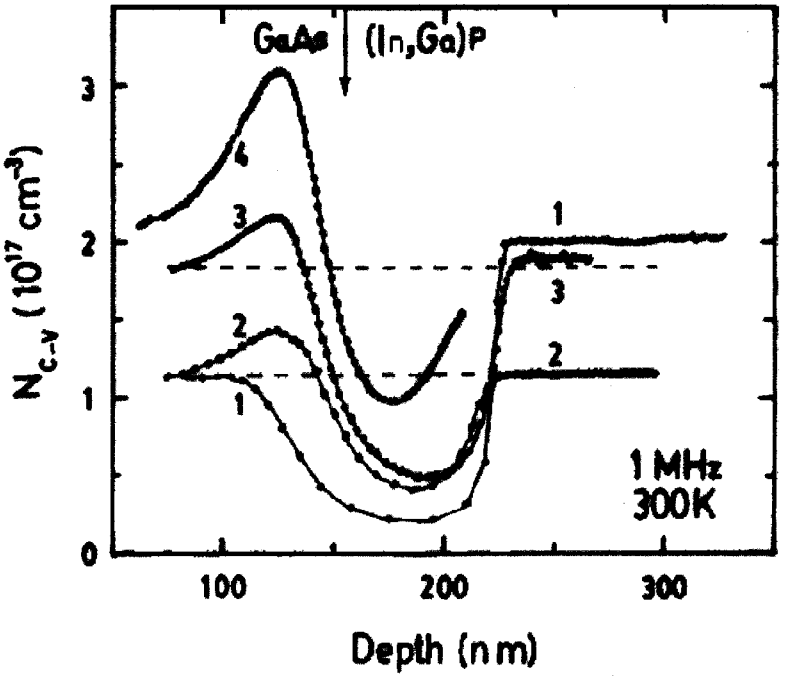

Fig. 1. Typical spatial distributions of the apparent carrier concentration $N_{C\text{-}V}$ for Si-doped GaAs/(In,Ga)P/GaAs isotype heterointerfaces grown by MOVPE. The samples 1,2,3 were grown with a V/III ratio of 70 at growth temperature 650°C, 580°C and 650°C respectively (curves 1,2,3). The sample of curve 4 was grown at 580°C with a V/III ratio of 140. The depth scales for curves 2 and 4 were shifted by -13 and -7 respectively, in order to compensate slight variations of the interface positions. Dashed lines denote the constant doping levels for depth profiles 2 and 3.

RESULTS AND DISCUSSION

For various Si-doped Ga-As-on-(In,Ga)P interfaces, the associated depth profiles of the apparent electron concentration $N_{C\text{-}V}$ are shown in Fig. 1. It is observed that the characteristics strongly depend on the growth temperature, the V/III ratio, and the substrate orientation. Accumulation of the carrier in the low band-gap material GaAs and depletion valley in the InGaP layer are only achieved for samples grown on the singular (001) surface. For such samples, the conduction band offset ΔE_C is found to be

0.20 eV. From the curves 1, 2, 3 and 4 in Fig. 1, we calculate carrier deficits at the interface of about 1×10^{12} cm^{-2}, 2.5×10^{11} cm^{-2}, 8×10^{11} cm^{-2} and less than 1×10^{11} cm^{-2} respectively. The electron deficit can be minimized by growth at 580^{o}C and higher V/III ratio (curve 4 in Fig. 1). In contrast, there is no accumulation of the carriers and a drastically enhanced carrier deficit at the interface with single-variant ordered (In,Ga)P (curve 1 in Fig. 1). For this interface, it is therefore not possible to determine the conduction band offset. ΔE_C. The position of the heterointerface is estimated at about 160 nm from the Schottky contact and the doping level of GaAs-on-InGaP layer as calculated from each end of the profile curve is nearly 1.1×10^{17} cm^{-3} [Blood and Orton 1992]. The lower electron concentration for GaAs in curve 1 is due to the lower doping efficiency during GaAs growth on the misoriented substrate.

In order to verify, whether the carrier deficit at the GaAs-on-(InGa)P interface originates from the deep interfacial levels, we performed DLTFS measurements close to the interface. Fig. 2 shows a series of deep-level spectra for the typical Si-doped GaAs/InGaP/GaAs isotype hetero-interface under different bias conditions. The figure exhibits a sequence of distinct DLTFS peaks labeled E_1-E_6, due to the electron emission from the traps. The peak heights of the levels E_1-E_5 are decreasing with the increasing depth until all the peaks disappear at reverse bias -3V, which practically exposes the InGaP layer. This clearly indicates that the electron levels E_1-E_5 originate from GaAs side. The activation energies associated with these levels are E_C - 0.20, E_C - 0.27, E_C - 0.4, E_C - 0.5 and E_C - 0.73 eV respectively. Peak E_5 is related to the well-known bulk level EL2 in MOVPE grown GaAs [Krispin *et al.* 2000] and E_6 appearing at higher reverse bias is typically observed in (In,Ga)P layers and is linked with the residual impurities in the MOVPE precursors [Hashizume *et al.* 1984]. However, we cannot compare the signatures of the peaks E_1-E_4 with the reported levels in the literature. It is, therefore, likely that these peaks may originate from the interfacial levels, which are responsible for the carrier deficit at the interface. Consequently, we estimated the total surface density N_{SS} by summing up the calculated values for each of the levels E_1-E_4, given by 1×10^{10} cm^{-2}, 3.5×10^{10} cm^{-2}, 1.4×10^{10} cm^{-2} and 3.5×10^{10} cm^{-2}. In this way we found that the total density (1.2×10^{11} cm^{-2}) of these so-called interfacial levels happens to be nearly one half of the estimated carrier deficit at the GaAs/InGaP interface (i.e. 2.50×10^{11} cm^{-2}) by *C-V* method. Accordingly, we are of the opinion that the large carrier deficit observed at the investigated interface could also be related to the interfacial levels in the lower half of the bandgap and/or to intrinsic electric field at the interface. Further work is therefore required to determine the origin of the large and growth-dependent carrier deficit at the Si-doped GaAs-on-InGaP interface.

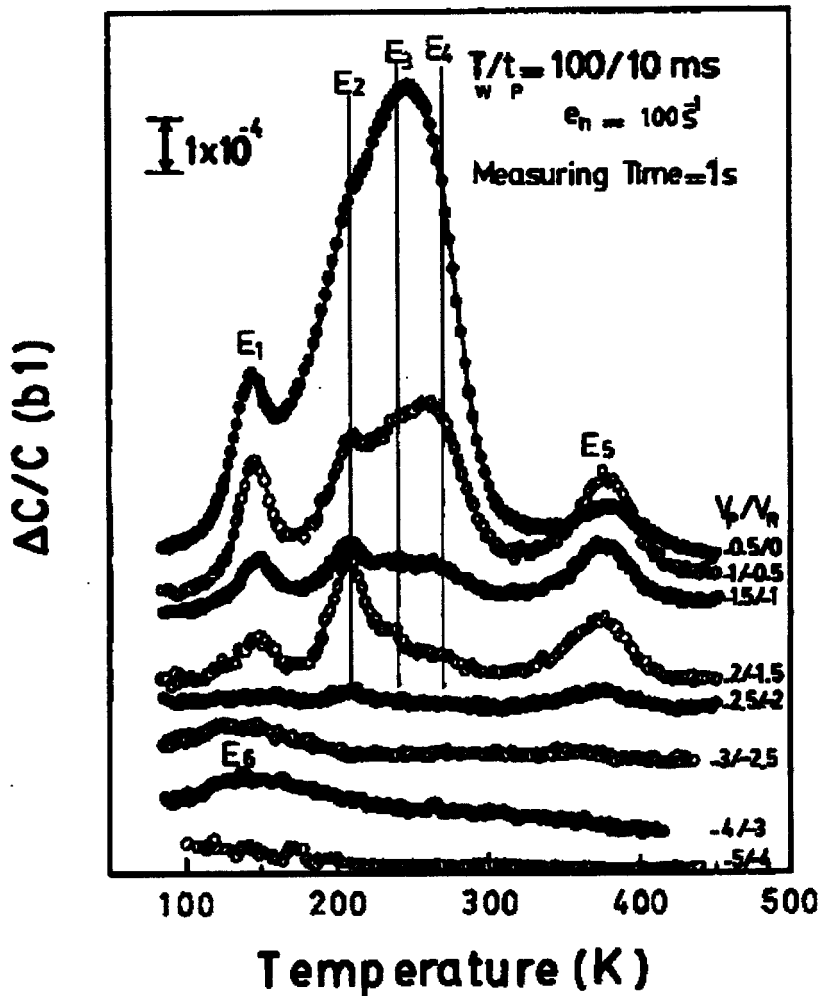

Fig. 2. Associated DLTFS spectra of a typical GaAs/(In,Ga)P/GaAs heterojunction grown at 580°C on a singular GaAs (001) substrate. The spectra are shifted vertically for clarity. The respective biasing conditions for each DLTFS signal are given along with the curves.

CONCLUSIONS

The electrical properties of Si-doped GaAs/(In,Ga)P/GaAs isotype heterointerfaces grown by MOVPE under different conditions have been carried out by using *C-V* and DLTFS measurement techniques. The salient features of our investigations are as what follows:

a) The characteristics strongly depend on the growth temperature, the V/III ratio, and the substrate orientation.

b) Observation of an accumulation of the carrier in the low bandgap material GaAs and depletion valley in InGaP layer clearly indicates the existence of well-defined heterointerface.
c) The conduction band discontinuity ΔE_C for the investigated layers is typically found to be 0.20 eV, which confirms the offset values reported in the literature [Biswas *et al.* 1990].
d) The carrier deficits at the various interfaces are estimated as 1×10^{12} cm^{-2}, 2.5×10^{11} cm^{-2}, 8×10^{11} cm^{-2} and less than 1×10^{11} cm^{-2} respectively.
e) The DLTFS study shows six electron levels at energy positions E_C - 0.20 eV, E_C - 0.27 eV, E_C - 0.40 eV, E_C - 0.50 eV, E_C - 0.73 eV and E_C - 0.34 eV respectively. Levels E_1-E_5 originate from GaAs side and the broad peak E_6 comes from the disordered InGaP layer.
f) Peak E_5 is related to the well-known EL2 level frequently observed in MOVPE grown GaAs material while a deep level having signatures similar to those of E_6 level has also been typically observed in (In,Ga)P layers and is linked with the residual impurities in the MOVPE precursors.
g) Levels E_1-E_4 are carefully attributed to the interfacial levels so as to justify the apparent carrier deficit found in the *C-V* measurements. But the total interfacial carrier density due to these levels happens to be half of the estimated carrier deficit.

Acknowledgements
The authors are thankful to Prof. Ploog, the Director Paul Drude Institute, Berlin, Germany for giving financial support to carry out the research activity. We are also grateful to E. Wiebeke for her technical assistance.

References

Biswas, D., Bebbar, N., Bhattacharya, P., Razeghi, M., Defour, M. and Omnes, F. (**1990**) *Appl. Phys. Lett.*, 56, 833.
Blood, P. and Orton, J.W. (**1992**) "The Electrical Characterization of Semiconductors: Majority Carriers and Electron States", Academic Press.
Cai, C., Nathan, M.I. and Lim, T.H. (**1999**) *Appl. Phys. Lett.*, 74, 720.
Chen, J.H., Sites, J.R., Spain, I.L., Hafich, M.J., Robinson, G.Y. (**1991**) *Appl. Phys. Lett.*, 58, 744.
Feng, S.L., Krynick, J., Donchev, V., Bourgoin, J.C., Forte-Poisson, M., Brylinski, C., Delage, S., Blanck, H. and Alaya, S. (**1993**) *Semicond. Sci. Technol.*, 8, 2092.
Hashizume, T., Ikeda, E., Akatsu, Y., Ohno, H. and Hasegawa, H. (**1984**) *Jpn. J. Appl. Phys.*, 23, Part 2, L296.
Kim, I.J., Cho, Y.H., Kim, K.S., Choe, K.D. and Lim, H. (**1996**) *Appl. Phys. Lett.*, 68, 3488.

Krispin, P., Asghar, M., Kanuer, A. and Kostial, H. (**2000**) *J. Crystal Growth*, 220, 220.

Krispin, P., Hey, R., Kostial, H. and Ploog, K.H. (**1998**) *J. Appl. Phys.* 83, 1496-1498.

Lee, T.W., Houston, P.A., Kumar, R., Yang, X.F., Hill, G., Hopkinson, M., and Claxton, P.A. (**1992**) *Appl. Phys. Lett.*, 60, 474.

O'Shea, J.J., Reaves, C.M., DenBaars, S.P., Chin, M.A. and Narayanamurti, V. (**1996**) *Appl. Phys. Lett.*, 69, 3022.

Rao, M.A., Cain, E.J., Kroemer, H., Long, S.I. and Babie, D.I. (**1987**) *J.Appl. Phys.*, 61, 643.

Tan, I.H., Sinder, G.L., Chang, L.D. and Hu, E.L. (**1990**) *J. Appl. Phys.*, 68, 4081.

Weiss, S. and Kassing, R. (**1988**) *Solid-State Electronics*, 31, 1733.

Zhang, H., Aoyogi, Y., Iwai, S. and Namba, S. (**1987**) *Appl. Phys. A*, 44, 273.

Zhu, Q.S. and Akasali, I. (**1992**) *Semicond. Sci. Technol.*, 7, 1441.